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IN THE CLAIMS

1. (Currently amended) A method for coding information in an electronic circuit, said circuit comprising at least two electrically coupled signal paths characterized in that the method comprises the steps of: determining an information bit to be encoded; encoding the information bit as a function of the relative delay between signals propagating on said paths when said signals make a transition from a first logic level to a second logic level; and producing as an output signal having a further logic level depending on said information bit according to the relative delay between said signals.

2. (Previously presented) The method according to claim 1, further comprising the step of: dividing a logical signal into two signals to be propagated on a respective one of said signal paths.

3. (Previously presented) The method according to claim 1, further comprising the step of: creating a reference signal being synchronized with the fastest signal propagating on either of said signal paths.

4. (Previously presented) The method according to claim 1, further comprising the step of: creating a relative delay between the signals propagating on said signal paths.

5. (Previously presented) The method according to claim 1, wherein the producing step is performed by means of a delay decoder.

6. (Currently amended) An electronic circuit for coding information, said circuit comprising at least two electrically coupled signal paths characterized in that the circuit comprises: means for determining an information bit to be encoded; means for encoding the information bit as a function of the relative delay between signals propagating on said paths when said signals make a transition from a first logic level to a second logic level; and means for producing as an output signal having a further logic level said information bit depending on the relative delay between said two signals.

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7. (Previously presented) The circuit according to claim 6, further comprising: means for dividing a logical signal into two signals to be propagated on a respective one of said signal paths.

8. (Previously presented) The circuit according to claim 6, further comprising: means for creating a reference signal (D) being synchronized with the fastest signal propagating on either of said signal paths.

9. (Previously presented) The circuit according to claim 6, further comprising: means for creating a relative delay between the signals propagating on said signal paths.

10. (Currently amended) The circuit according to ~~any of~~ claims 6, wherein the producing means comprise a delay decoder.